TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application No.	09/475,487
Filing Date	December 30, 1999
First Named Inventor	Azar Assadi
Art Unit	2612
Examiner Name	Myers, Paul W.
Total Number of Pages in This Submission	55
Attorney Docket Number	42390P6880

ENCLOSURES *(check all that apply)*

- [X] Fee Transmittal Form
  - [X] Fee Attached
- [ ] Amendment / Response
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
  - [ ] PTO/SB/08
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Basic Filing Fee
  - [ ] Declaration/POA
- [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s)
- [ ] After Allowance Communication to Group
- [ ] Appeal Communication to Board of Appeals and Interferences
- [X] Appeal Communication to Group **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [X] Other Enclosure(s) *(please identify below):*

Return receipt postcard

Remarks

APPEAL BRIEF

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Steven Laut, Reg. No. 47,736 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	
Date	July 7, 2004

CERTIFICATE OF MAILING/TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Typed or printed name	**Jean Svoboda**		
Signature		Date	**July 7, 2004**

FEE TRANSMITTAL for FY 2004

Effective 01/01/2004. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT ($) 330.00

Complete if Known	
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METHOD OF PAYMENT *(check all that apply)*

☒ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☒ Deposit Account

Deposit Account Number: 02-2666

Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

The Commissioner is authorized to: *(check all that apply)*

☐ Charge fee(s) indicated below ☒ Credit any overpayments

☒ Charge any additional fee(s) or underpayment of fees as required under 37 CFR §§ 1.16, 1.17, 1.18 and 1.20.

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES

	Extra Claims		Fee from below		Fee Paid
Total Claims		- 25** =		X =	
Independent Claims		- 4 =		X =	
Multiple Dependent				=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple Dependent claim, if not paid
1204	86	2204	43	**Reissue independent claims over original patent
1205	18	2205	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

***or number previously paid, if greater, For Reissues, see below*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920 *	1804	920 *	Requesting publication of SIR prior to Examiner action	
1805	1,840 *	1805	1,840 *	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1404	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	330.00
1403	290	2403	145	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	1809	385	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR § 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify)

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 330.00

SUBMITTED BY

Complete (if applicable)

Name *(Print/Type)*	Steven Laut	*Registration No. (Attorney/Agent)*	47,736	*Telephone*	(310) 207-3800
Signature				*Date*	07/07/04

Based on PTO/SB/17 (10-03) as modified by Blakely, Sokoloff, Taylor & Zafman (wtr) 02/10/2004.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Our Ref. No.: 042390.P6880

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

Azar Assadi

Serial No. 09/475,487

Filed: December 30, 1999

For: **COLOR IMAGE SENSOR WITH INTEGRATED BINARY OPTICAL ELEMENTS**

Examiner: Myers, Paul W.

Art Unit: 2612

APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
Post Office Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

Applicants submit, in triplicate, the following Appeal Brief pursuant to 37 C.F.R. § 1.192 for consideration by the Board of Patent Appeals and Interferences. Applicants authorize the Commissioner to charge a payment in the amount of $330.00 to cover the cost of filing the opening brief as required by 37 C.F.R. § 1.17(c) to Deposit Account No. 02-2666.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

07/15/2004 HALI11 00000037 09475487
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TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

Azar Assadi, the party named in the caption, assigned her rights to that disclosed in the subject application through an assignment recorded on March 27, 2000 (010645/0170) to Intel Corporation of Santa Clara, California. Thus, as owner at the time the brief is being filed, Intel Corporation of Santa Clara, California, is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-26 are pending in the present application. A final Office Action was mailed on February 17, 2004. A notice of Appeal was filed by mail on May 4, 2004, received by the U.S.P.T.O. on May 7, 2004 as evidenced from a received self-addressed postcard. No further action has been received from the Examiner as of this date.

IV. STATUS OF AMENDMENTS

On October 23, 2003, Applicant filed an amendment in response to an August 28, 2003 Office Action (non-final) for consideration by the Examiner. The Examiner issued a Final Office Action on February 17, 2004. The claims remain as amended in the October 23, 2003 response (the status indicators of the claims have been updated to their current status).

V. SUMMARY OF THE INVENTION

With the below listed embodiments, a protection layer is used to protect the diode on top and also for integrating micro-optics elements for producing color schemes. The integration of optics, electronics and photonics components increases sensor processing capabilities and reduces cost reducing process steps, and reduces detection area by integrating the grating with the protective layer. The integrated

protective layer, therefore, protects from environmental stresses (such as humidity and scratches), produces color and also filters.

One embodiment of the present invention concerns an integrated pixel sensor structure including a light sensitive diode having a transparent conductor. A protective layer is placed above the transparent conductor. The protective layer includes a set of diffraction grating elements for producing complementary colors.

Another embodiment of the present invention concerns a system including an integrated pixel sensor structure having a light sensitive diode including a transparent conductor. A protective layer is placed above the transparent conductor. The protective layer includes a set of diffraction grating elements for producing complementary colors. A post capture signal processing unit is connected to the integrated pixel sensor.

Yet another embodiment of the present invention concerns a method, that includes providing a light sensitive element, placing a transparent conductor above the light sensitive element, and placing a protective layer above the transparent conductor. The protective layer includes a set of diffraction grating elements for producing complementary colors.

Still another embodiment of the present invention concerns an integrated circuit die including an image sensing area of the die having many light-sensitive diodes formed above a metalization layer of the die, and a protective layer of the die. The protective layer is to protect the many diodes and is shaped as a diffraction grating.

VI. ISSUES

The issues involved in this appeal are as follows:

Under 35 U.S.C. § 103(a):

A. Claims 1-16 as being unpatentable over US 2003/0138988 to Murakami et al. ("Murakami") in view of U.S. Patent No. 5,976,907 issued to Shigeta et al. ("Shigeta") in further view of U.S. Patent No. 5,682,265 issued to Farn et al. ("Farn").

B. Claims 17-19 and 21-26 as being unpatentable over U.S. Patent No. 6,501,065 issued to Uppal et al. ("Uppal") in view of US 2003/0138988 to Murakami et al. ("Murakami") in view of U.S. Patent No. 5,600486 issued to Gal et al. ("Gal").

C. Claim 20 as being unpatentable over Uppal in view of Murakami in view of Gal in view of U.S. Patent No. 6,163,386 issued to Kobayashi et al. ("Kobayashi").

VII. GROUPING OF CLAIMS

Applicants contend that the claims can be divided into **five** groups and that each group of claims is separately patentable for the reasons asserted below and in the Arguments. These groups are as follows:

Group I	**Claims 1-4**
Group II	**Claims 5-8**
Group III	**Claims 13-16**
Group IV	**Claims 17-26**

The claims of Group I are integrated pixel sensor structure claims and apparatus claims. The claims of Group II are system claims. The claims of Group III are method claims. The claims of Group IV are integrated circuit die claims. Claims 1, 5, 9, 13 and 17 are each independent claims. The independent claims of each group contain distinguishable limitations from one another and also from the prior art at issue (see below and Argument section), and thus, each group's independent claims, and its associated dependent claims, are separately patentable. Since the distinguishable

independent claims and associated dependent claims are separately grouped, each group is separately patentable. Since each group is separately patentable, and each group contains at least one independent claim and associated dependent claims, each group's independent claim(s) and associated dependent claims stands or falls together. Further, see the discussion below and also the Argument section for additional reasons how each group is separately patentable, and therefore, why each group of claims should stand or fall together.

Claim 1 contains the limitations of "[a]n integrated pixel sensor structure comprising: ..." Claim 9 contains the limitations of "[a]n apparatus comprising:..." Since no other independent claims (i.e. claims 5, 13 and 17) relate to an integrated pixel sensor structure or Apparatus containing the same limitations as claims 1 and 9, **Group I is separately patentable** (See also arguments below). **Since claims 2-4 depend directly or indirectly on claim 1, and claims 10-12 depend directly or indirectly on claim 9, claims 1-4 and 9-12 stand or fall together.**

Claim 5 contains the limitations of "[a] system comprising: an integrated pixel sensor structure... and a post capture signal processing unit coupled to the integrated pixel sensor." **Since no other independent claims (i.e., claims 1, 9, 13 and 17) relates to a system containing the same limitations as claim 5,** Group II is separately patentable **(See also arguments below).** Since claims 6-8 directly or indirectly depend on claim 5, claims 5-8 stand or fall together.

Claim 13 contains the limitations of "[a] method comprising: ..." Since no other independent claims (i.e., claims 1, 5, 9 and 17) relates to a method containing the same limitations as claim 13, **Group III is separately patentable** (See also arguments below). **Since claims 14-16 directly or indirectly depend on claim 13, claims 13-16 stand or fall together.**

Claim 17 contains the limitations of "[a]n integrated circuit die comprising: ..." Since no other independent claims (i.e., claims 1, 5, 9 and 13) relates to an integrated circuit die containing the same limitations as claim 17, **Group IV is separately patentable** (See also arguments below). **Since claims 18-26 directly or indirectly depend on claim 17, claims 17-26 stand or fall together.**

VIII. ARGUMENT

A. It is asserted in the Final Office Action that Claims 1-16 as being unpatentable over Murakami in view of Shigeta in further view of Farn. This rejection is respectfully traversed. The following discussion sets forth in detail Applicant's analysis with respect to the patentability of claims 1-16.

The above claims relate to an integrated pixel sensor structure, a system, an apparatus and a method where a diode on top ("DOT") image sensor has a protective layer (a low temperature deposition layer that protects against environmental stress, such as humidity and scratches, and antireflection (AR)) that also includes grating (micro-optic elements) for producing an RGB color scheme.

According to MPEP 2141.02 "[i]n determining the differences between the prior art and the claims, the question under 35 U.S.C. 103 is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious. (Stratoflex, Inc. v. Aeroquip Corp., 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); Schenck v. Nortron Corp., 713 F.2d 782, 218 USPQ 698 (Fed. Cir. 1983)). Distilling an invention down to the 'gist' or 'thrust' of an invention disregards the requirement of analyzing the subject matter "as a whole." (W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984))." Applicant asserts that the concept of using an image sensor having a protective layer with micro-optics (gratings) within the protective layer must be looked at "as a whole," not just a "gist: or "thrust" of improving image sensor processes by including one layer for producing color, protection and filtering.

Further, under MPEP 2142 "[t]o establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable

expectation of success must both be found in the prior art, and not based on applicant's disclosure." (In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)).

Applicant asserts that a *prima facie* case of obviousness has not been met. First, there is neither suggestion nor motivation in Murakami, Shigeta, nor Farn to have a sensor including a protection layer incorporating diffraction grating elements. The Office Action correctly asserts on page 3 that Murakami "does not disclose (*sic.*) protective layer including a set of diffraction grating elements for producing complementary colors." The Office Action then looks to Shigeta, which shows a solid state imaging device, and particularly one which has a second flattening layer (15) on the surface of a color filter (14). Shigeta, col. 6, line 55 to col. 7, line 4.

The Office Action concludes, on page 4, that it would have been obvious to modify the teachings of Murakami and Shigeta so as to add a diffraction grating that is capable of producing complementary colors, because Farn discloses an apparatus for dispersing visible light spectrum into primary color bands, using a diffraction grating (rather than filters of particular colors). Farn, col. 1, lines 29-35 and lines 60-65. Applicant, however, respectfully disagrees that it would have been obvious to modify Murakami and Shigeta in accordance with Farn, because although both Murakami and Shigeta are directed to image sensing devices, the invention in Farn relates to improving the energy efficiency of a display device. Farn, col. 1, lines 9-26. In Farn, the diffraction gratings are used (instead of small filters) to improve the energy efficiency of display devices such as cathode ray tube displays and liquid crystal displays. Neither Murakami nor Shigeta is concerned with display devices. Moreover, there is no teaching or suggestion in Murakami or Shigeta that the energy efficiency of the imaging device is a problem. Lastly, even if such a problem were suggested, there is nothing to suggest that the color filters of Shigeta are the "wasteful" culprits. It would not have been obvious to modify either Murakami or Shigeta in accordance with any diffraction grating teachings of Farn as the prior art references, considered as a whole, simply do not suggest the desirability and thus the obviousness of making the combination. Also, if the prior art references are combined there is no showing of a reasonable expectation of success.

Therefore, since there is no suggestion at all, nor motivation to modify the references or combine the three to arrive at Applicant's claimed invention, and the prior art references do not "teach or suggest all the claim limitations," a *prima facie* obviousness rejection has not been made.

Further, according to MPEP 2143.01, "[t]he mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." (In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990)). Nowhere in Murakami or Shigeta is there a suggestion of the desire to have a protective layer including diffraction grating elements, as asserted in claims 1, 5, 9 and 13. And, just by looking at Murakami, Shigeta and Farn there is not a suggestion of the desire to combine the prior art. Nowhere in either Murakami or Shigeta is a mention regarding diffraction gratings, or using a same layer for protection, color production and filtering.

Moreover, according to MPEP 2142, [t]o reach a proper determination under 35 U.S.C. 103, the examiner must step backward in time and into the shoes worn by the hypothetical 'person of ordinary skill in the art' when the invention was unknown and just before it was made. In view of all factual information, the examiner must then make a determination whether the claimed invention 'as a whole' would have been obvious at that time to that person. Knowledge of applicant's disclosure must be put aside in reaching this determination, yet kept in mind in order to determine the 'differences,' conduct the search and evaluate the 'subject matter as a whole' of the invention. The tendency to resort to 'hindsight' based upon applicant's disclosure is often difficult to avoid due to the very nature of the examination process. However, impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art." Applicant submits that without Applicant's disclosure, no thought, whatsoever, would have been made to design an image sensor structure having a protective layer including diffraction gradients included in the protective layer. Applicant's concept was never considered in the art. Further, nowhere in the Office Action (see page 4 of the Office Action) is a motivation given for the combination of the prior art. It is only asserted in the Office Action that

the three prior art documents each include an element of Applicant's claims 1, 5, 9 and 13, without any suggestion for combining these elements, nor motivation.

As discussed above, neither Murakami, Shigeta, Farn, or the combination of the three, teach, disclose or suggest all the limitations contained in Applicant's claims 1, 5, 9 and 13. Since neither Murakami, Shigeta nor Farn teach, disclose or suggest the limitations contained in Applicant's claims 1, 5, 9 and 13, it would not have been obvious to one of ordinary skill in the art to combine the teachings of Murakami in view of Shigeta in further view of Farn. Moreover, without impermissible hindsight one skilled in the art would not have looked to combine the teachings of Farn with that of Murakami and Shigeta.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejection is respectfully requested.

B. It is asserted in the Final Office Action that Claims 17-19 and 21-26 are unpatentable over Uppal in view of Murakami in view of Gal.

Claims 18-19 and 21-26 directly or indirectly depend from Applicant's claim 17.

As asserted above in section VIII(A), Murakami does not teach, disclose or suggest an image sensor structured with a protective layer including diffraction grating elements. Uppal discloses an image sensor having pin photodiodes placed on top CMOS circuitry. Applicant agrees with the assertion in the Office Action on page 6 that neither Uppal nor Murakami disclose the protective layer is shaped as diffraction grating. Gal discloses a color separation microlens where a single micro-optical element is made up of color separation grating integrated with a refractive lens. The only assertion in the Office Action of why Gal is relied upon is that "grating can be used to separate colors of a spectral band by diffraction." Nowhere in the Office Action is it pointed out where a suggestion or motivation would be to combine the prior art references.

Applicant asserts that a *prima facie* case of obviousness has not been met with respect to claim 17. First, there is neither suggestion nor motivation in Murakami,

Uppal nor Gal to have the protective layer of an integrated circuit die having a plurality of light-sensitive diodes formed above a metalization layer, where the protective layer is shaped as diffraction grating. Murakami, Uppal and Gal simply do not teach, disclose, nor suggest such limitations. Thus, it would not have been obvious to modify Murakami, Uppal or Gal as the prior art references, considered as a whole, simply do not suggest the desirability and thus the obviousness of making the combination. Also, if the prior art references are combined there is no showing of a reasonable expectation of success.

Without exploring Applicant's specification, one skilled in the art would not have thought to have the protective layer of an integrated circuit die having a plurality of light-sensitive diodes formed above a metalization layer, where the protective layer is shaped as diffraction grating.

Therefore, since there is no suggestion at all, nor motivation to modify the references or combine the three to arrive at Applicant's claimed invention, and the prior art references do not "teach or suggest all the claim limitations," a *prima facie* obviousness rejection has not been made with respect to Applicant's claim 17. Further, without impermissible hindsight one skilled in the art would not have thought to combine the prior art references to have the protective layer of an integrated circuit die having a plurality of light-sensitive diodes formed above a metalization layer, where the protective layer is shaped as diffraction grating. Additionally, the claims that directly or indirectly depend from Applicant's claim 17, namely claims 18-19 and 21-26, are also not obvious over Uppal in view of Murakami in view of Gal for the same reasons.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejection is respectfully requested.

C. It is asserted in the Final Office Action that Claim 20 is unpatentable over Uppal in view of Murakami in view of Gal in view of Kobayashi.

Applicant's Claim 20 indirectly depends on Claim 17, which is discussed in section VIII(B) regarding Uppal, Murakami and Gal.

Kobayashi discloses a photoelectric conversion device for reading signals in succession from multiple photoelectric converting. Neither Uppal, Murakami, Gal, Kobayashi, nor the combination of the four teach, disclose or suggest to have the protective layer of an integrated circuit die having a plurality of light-sensitive diodes formed above a metalization layer, where the protective layer is shaped as diffraction grating. None of the prior art references contain any suggestion or motivation to combine the teachings to arise at Applicant's claimed invention.

Since there is no suggestion at all, nor motivation to modify the references or combine the four to arrive at Applicant's claimed invention, and the prior art references do not "teach or suggest all the claim limitations," a *prima facie* obviousness rejection has not been made with respect to Applicant's claim 17. Further, without impermissible hindsight one skilled in the art would not have thought to combine the prior art references to have the protective layer of an integrated circuit die having a plurality of light-sensitive diodes formed above a metalization layer, where the protective layer is shaped as diffraction grating. Additionally, the claim that indirectly depends from Applicant's claim 17, namely claim 20, is also not obvious over Uppal in view of Murakami in view of Gal in view of Kobayashi for the same reasons.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejection is respectfully requested.

IX. CONCLUSION AND RELIEF

Based on the foregoing, Applicant requests that the Board overturn the rejection of all pending claims and hold that all of the claims of the present application are allowable.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Dated: July 7, 2004

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CERTIFICATE OF MAILING:

I hereby certify that this correspondence is being deposited as First Class Mail, with sufficient postage, with the United States Postal Service in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450 on July 7, 2004.

Jean Svoboda July 7, 2004

X. APPENDIX

The claims involved in this Appeal are as follows:

1. (Original) An integrated pixel sensor structure comprising:

a light sensitive diode including a transparent conductor; and,

a protective layer placed above the transparent conductor, the protective layer including a set of diffraction grating elements for producing complementary colors.

2. (Original) The structure of claim 1, where the protective layer includes anti-reflection properties.

3. (Previously Presented) The structure of claim 1, where the light sensitive diode is compatible with and the protective layer is a material suitable for use with metal oxide semiconductor fabrication processes.

4. (Original) The structure of claim 1, where the set of diffraction grating elements include a set of four step echelon grating elements.

5. (Original) A system comprising:

an integrated pixel sensor structure having:

a light sensitive diode including a transparent conductor; and,

a protective layer placed above the transparent conductor, the protective layer including a set of diffraction grating elements for producing complementary colors; and,

a post capture signal processing unit coupled to the integrated pixel sensor.

6. (Original) The system of claim 5, where the protective layer includes anti-reflection properties.

7. (Previously Presented) The system of claim 5, where the protective layer is of a sol gel material suitable for fabrication processes that are compatible with the light sensitive diode.

8. (Original) The system of claim 5, where the set of diffraction grating elements include a set of four step echelon grating elements.

9. (Original) An apparatus comprising:

a light sensitive means;

a transparent conductor means displaced above the light sensitive means; and,

a protective layer means placed above the transparent conductor means, the protective layer means including a set of diffraction grating means for producing complementary colors.

10. (Original) The apparatus of claim 9, where the protective layer means includes anti-reflection properties.

11. (Previously Presented) The apparatus of claim 9, where the protective layer means is a material suitable for metal oxide semiconductor integrated circuit fabrication processes.

12. (Original) The apparatus of claim 9, where the set of diffraction grating means include a set of four step echelon grating elements.

13. (Original) A method comprising:

providing a light sensitive element;

placing a transparent conductor above the light sensitive element; and,

placing a protective layer above the transparent conductor, the protective layer including a set of diffraction grating elements for producing complementary colors.

14. (Original) The method of claim 13, where placing the protective layer includes placing a material with anti-reflection properties above the transparent conductor.

15. (Original) The method of claim 13, where placing the protective layer includes placing a material suitable for fabrication processes that are compatible with the light sensitive element.

16. (Original) The method of claim 13, where the set of diffraction grating elements include a set of four step echelon grating elements.

17. (Previously Presented) An integrated circuit die comprising:

an image sensing area of the die having a plurality of light-sensitive diodes formed above a metalization layer of the die; and

a protective layer of the die, wherein the protective layer is to protect the plurality of diodes and is shaped as a diffraction grating.

18. (Previously Presented) The integrated circuit die of claim 17 wherein the plurality of diodes have amorphous silicon as their photo-active material.

19. (Previously Presented) The integrated circuit die of claim 18 wherein each of the plurality of diodes has a n-i-p structure.

20. (Previously Presented) The integrated circuit die of claim 19 wherein each of the n and p portions of the n-i-p structure is thin relative to the i portion.

21. (Previously Presented) The integrated circuit die of claim 18 wherein the plurality of diodes have a transparent conductor made of an indium tin oxide (ITO) layer that forms a top contact of the plurality of diodes.

22. (Previously Presented) The integrated circuit die of claim 18 wherein the plurality of diodes have a transparent conductor that forms a top contact of the plurality of diodes and wherein the protective layer has a low enough deposition temperature so as not to environmentally stress the transparent conductor.

23. (Previously Presented) The integrated circuit die of claim 17 wherein the protective layer has anti-reflective properties to act as an antireflective filter for the image sensing area of the die.

24. (Previously Presented) The integrated circuit die of claim 22 wherein the diffraction grating is designed to impart RGB color sensing to the image sensing area of the die.

25. (Previously Presented) The integrated circuit die of claim 22 wherein the protective layer is made of a sol-gel material.

26. (Previously Presented) The integrated circuit die of claim 17 wherein the plurality of diodes and the protective layer are compatible with a metal oxide semiconductor (MOS) fabrication process.